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Text Part Number: 78EE117C99-1114823145

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## 1.4 bcc 0.12.0

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Format: <http://www.debian.org/doc/packaging-manuals/copyright-format/1.0/>

Upstream-Name: bcc

Source: <https://github.com/iovisor/bcc>

Files: \*

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## 1.5 libxml 2.9.10

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## 1.6 httpparser 2.8.1

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## 1.7 x-net 0.0.0-20201207224615-747e23833adb

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# 1.8 llvm 8.0.1

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```
; RUN: opt -consthoist -S -o - %s | FileCheck %s
```

```
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
```

```
target triple = "thumbv6m-none--musleabi"
```

```
; Check that for i8 type, the maximum legal offset is 31.
```

```
; Also check that a constant used as value to be stored rather than
```

```
; pointer in a store instruction is hoisted.
```

```
; CHECK: foo_i8
```

```
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
```

```
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
```

```
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
```

```

; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo

```

```
@goo = global i8* undef
```

```

define void @foo_i8() {
entry:
%0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
%1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
%2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
%3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
%4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

```

```
; Check that for i16 type, the maximum legal offset is 62.
```

```
; CHECK: foo_i16
```

```
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
```

```

; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

```

```

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}

```

```

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*

```

```
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4
```

```
define void @foo_i32() {  
entry:  
%0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4  
%1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4  
%2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4  
%3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4  
%4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4  
%5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4  
ret void  
}
```

```
# People who have agreed to one of the CLAs and can contribute patches.
```

```
# The AUTHORS file lists the copyright holders; this file
```

```
# lists people. For example, Google employees are listed here
```

```
# but not in AUTHORS, because Google holds the copyright.
```

```
#
```

```
# Names should be added to this file only after verifying that
```

```
# the individual or the individual's organization has agreed to
```

```
# the appropriate Contributor License Agreement, found here:
```

```
#
```

```
# https://developers.google.com/open-source/cla/individual
```

```
# https://developers.google.com/open-source/cla/corporate
```

```
#
```

```
# The agreement for individuals can be filled out on the web.
```

```
#
```

```
# When adding J Random Contributor's name to this file,
```

```
# either J's name or J's organization's name should be
```

```
# added to the AUTHORS file, depending on whether the
```

```
# individual or corporate CLA was used.
```

```
#
```

```
# Names should be added to this file as:
```

```
# Name <email address>
```

```
#
```

```
# Please keep the list sorted.
```

```
Albert Pretorius <pretoalb@gmail.com>
```

```
Arne Beer <arne@twobeer.de>
```

```
Billy Robert O'Neal III <billy.oneal@gmail.com> <bion@microsoft.com>
```

```
Chris Kennelly <ckennelly@google.com> <ckennelly@ckennelly.com>
```

```
Christopher Seymour <chris.j.seymour@hotmail.com>
```

```
David Coeurjolly <david.coeurjolly@liris.cnrs.fr>
```

```
Deniz Evrenci <denizevrenci@gmail.com>
```

```
Dominic Hamon <dma@stripsock.com> <dominic@google.com>
```

```
Dominik Czarnota <dominik.b.czarnota@gmail.com>
```

```
Eric Fiselier <eric@efcs.ca>
```

```
Eugene Zhuk <eugene.zhuk@gmail.com>
```

```
Evgeny Safronov <division494@gmail.com>
```

Felix Homann <linuxaudio@showlabor.de>  
Ismael Jimenez Martinez <ismael.jimenez.martinez@gmail.com>  
Jern-Kuan Leong <jernkuan@gmail.com>  
JianXiong Zhou <zhoujianxiong2@gmail.com>  
Joao Paulo Magalhaes <joaoppmagalhaes@gmail.com>  
John Millikin <jmillikin@stripe.com>  
Jussi Knuutila <jussi.knuutila@gmail.com>  
Kai Wolf <kai.wolf@gmail.com>  
Kishan Kumar <kumar.kishan@outlook.com>  
Kaito Udagawa <umireon@gmail.com>  
Lei Xu <eddyxu@gmail.com>  
Matt Clarkson <mattyclarkson@gmail.com>  
Maxim Vafin <maxvafin@gmail.com>  
Nick Hutchinson <nshutchinson@gmail.com>  
Oleksandr Sochka <sasha.sochka@gmail.com>  
Pascal Leroy <phl@google.com>  
Paul Redmond <paul.redmond@gmail.com>  
Pierre Phaneuf <pphaneuf@google.com>  
Radoslav Yovchev <radoslav.tm@gmail.com>  
Raul Marin <rmrodriguez@cartodb.com>  
Ray Glover <ray.glover@uk.ibm.com>  
Robert Guo <robert.guo@mongodb.com>  
Roman Lebedev <lebedev.ri@gmail.com>  
Shuo Chen <chenshuo@chenshuo.com>  
Tobias Ulvgrd <tobias.ulvgard@dirac.se>  
Tom Madams <tom.ej.madams@gmail.com> <tmadams@google.com>  
Yixuan Qiu <yixuanq@gmail.com>  
Yusuke Suzuki <utatane.tea@gmail.com>  
Zbigniew Skowron <zbychs@gmail.com>  
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-----

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\*/

; NOTE: Assertions have been autogenerated by utils/update\_analyze\_test\_checks.py

; RUN: opt < %s -cost-model -analyze -mtriple=x86\_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX

; RUN: opt < %s -cost-model -analyze -mtriple=x86\_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256

; RUN: opt < %s -cost-model -analyze -mtriple=x86\_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256() "min-legal-vector-width"="256" {

; VEC256-LABEL: 'zext256'

; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>

```

; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>

```

```

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'sext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x

```

```

i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>

```

```

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
ret void
}

define internal void @innerNoAttribute() {
ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
call void @innerLarge()
ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
call void @innerLarge()
ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
call void @innerSmall()
ret void
}

```

```

}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:

; First, extend each i32 to i64
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.

```

```

define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}
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```

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```
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.
```

```
declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
  ret fp128 %res
; CHECK-LABEL: TestSelect:
; CHECK      movaps 16(%rsp), %xmm1
; CHECK-NEXT  callq __subtf3
; CHECK-NEXT  testl %ebx, %ebx
; CHECK-NEXT  jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT  movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT  addq $32, %rsp
; CHECK-NEXT  popq %rbx
; CHECK-NEXT  retq
}
```

```
define fp128 @TestFabs(fp128 %a) {
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
; CHECK-LABEL: TestFabs:
; CHECK      andps .LCPI1_0(%rip), %xmm0
; CHECK-NEXT  retq
}
```

```
define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
  ret fp128 %res
}
```



```

; CHECK-LABEL: TestCopysign:
; CHECK    andps .LCPI2_1(%rip), %xmm0
; CHECK-NEXT orps %xmm1, %xmm0
; CHECK-NEXT retq
}

define fp128 @TestFneg(fp128 %a) {
    %mul = fmul fp128 %a, %a
    %res = fsub fp128 0xL00000000000000008000000000000000, %mul
    ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK    movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}

```

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```
; RUN: llc -march=hexagon < %s
```

```
; REQUIRES: asserts
```

```
; The two loads based on %struct.0, loading two different data types  
; cause LSR to assume type "void" for the memory type. This would then  
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.
```

```
target triple = "hexagon"
```

```
%struct.0 = type { i8*, i8, %union.anon.0 }
```

```
%union.anon.0 = type { i8* }
```

```
define hidden fastcc void @fred() unnamed_addr #0 {
```

```
entry:
```

```
br i1 undef, label %while.end, label %while.body.lr.ph
```

```
while.body.lr.ph:                                ; preds = %entry
```

```
br label %while.body
```

```
while.body:                                     ; preds = %exit.2, %while.body.lr.ph
```

```
%lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
```

```

switch i32 undef, label %exit [
  i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
]

```

```

sw.bb.i:                                ; preds = %while.body
unreachable

```

```

sw.bb3.i:                                ; preds = %while.body
unreachable

```

```

exit:                                    ; preds = %while.body
switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
]

```

```

sw.bb.i17:                               ; preds = %exit
%0 = bitcast %struct.0* %lshr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

```

```

sw.bb3.i20:                              ; preds = %exit
%2 = bitcast %struct.0* %lshr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable

```

```

exit.2:                                   ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lshr.iv, i32 1
br label %while.body

```

```

while.end:                                ; preds = %entry
ret void
}

```

```

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }

```

```

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

```

```

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vl,avx512bw,avx512dq,prefer-256-bit |
FileCheck %s

```

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: add256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1

```







```

%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-
width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-
width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vzeroupper

```

```

; CHECK-NEXT:  retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT:  movl %edx, %eax
; CHECK-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:  xorl %ecx, %ecx
; CHECK-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:  vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:  .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT:  vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT:  vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT:  vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:  vpadd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:  vpmovsxbw 16(%rsi,%rcx), %ymm3
; CHECK-NEXT:  vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT:  vpadd %ymm2, %ymm3, %ymm2

```

```

; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax
; CHECK-NEXT: jne .LBB8_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT: vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

```

vector.body:

```

%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

```

middle.block:

```

%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf

```

```

%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

```

```

define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-
width"="512" {

```

```

; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT:  movl %edx, %eax
; CHECK-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:  xorl %ecx, %ecx
; CHECK-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:  .p2align 4, 0x90
; CHECK-NEXT: .LBB9_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:  vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:  vpadd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB9_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT:  vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vpslufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vpslufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vmovd %xmm0, %eax

```



```

%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

```

```
@a = global [1024 x i8] zeroinitializer, align 16
```

```
@b = global [1024 x i8] zeroinitializer, align 16
```

```
define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: sad_16i8_256:
```

```
; CHECK: # %bb.0: # %entry
```

```
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
```

```
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
```

```
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
```

```
; CHECK-NEXT: .p2align 4, 0x90
```

```
; CHECK-NEXT: .LBB10_1: # %vector.body
```

```
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
```

```
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
```

```
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
```

```
; CHECK-NEXT: vpadd %ymm1, %ymm2, %ymm1
```

```
; CHECK-NEXT: addq $4, %rax
```

```
; CHECK-NEXT: jne .LBB10_1
```

```
; CHECK-NEXT: # %bb.2: # %middle.block
```

```
; CHECK-NEXT: vpadd %ymm0, %ymm1, %ymm0
```

```
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
```

```
; CHECK-NEXT: vpadd %ymm1, %ymm0, %ymm0
```

```
; CHECK-NEXT: vpshufd { {.*#+} } xmm1 = xmm0[2,3,0,1]
```

```
; CHECK-NEXT: vpadd %ymm1, %ymm0, %ymm0
```

```
; CHECK-NEXT: vpshufd { {.*#+} } xmm1 = xmm0[1,1,2,3]
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vmovd %xmm0, %eax
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
entry:
```

```
br label %vector.body
```

```
vector.body:
```

```
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
```

```
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
```

```
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
```

```
%1 = bitcast i8* %0 to <16 x i8>*
```

```
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
```

```
%2 = zext <16 x i8> %wide.load to <16 x i32>
```

```
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
```

```
%4 = bitcast i8* %3 to <16 x i8>*
```

```
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
```

```
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
```

```
%6 = sub nsw <16 x i32> %2, %5
```

```

%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

```

middle.block:

```

%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

```

```

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {

```

```

; CHECK-LABEL: sad_16i8_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB11_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT: vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB11_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT: vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpadd %zmm1, %zmm0, %zmm0

```

```

; CHECK-NEXT: vpsfud { {.#+} } xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vpsfud { {.#+} } xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
br label %vector.body

vector.body:
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4

```



```

%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2

```

```

; CHECK-NEXT:   vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:   vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:   vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:   vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:   vmovaps %ymm3, (%rdi)
; CHECK-NEXT:   vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:   vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm1, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

```

```

%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:  vcvt dq2pd %ymm0, %zmm1
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:  vcvt dq2pd %ymm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:  vmovaps %zmm1, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvt tps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvt tps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvt tps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq

```

```

%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: mul256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpunpckhbw {{.*#+}} %ymm4 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13
],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ym
m0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[

```

```

31]
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-NEXT: vmovdqa {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-NEXT: vpand %ymm5, %ymm4, %ymm4
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-NEXT: vpackuswb %ymm4, %ymm0, %ymm0
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm2 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[31]
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[31]
; CHECK-NEXT: vpmullw %ymm2, %ymm4, %ymm2
; CHECK-NEXT: vpand %ymm5, %ymm2, %ymm2
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-NEXT: vpackuswb %ymm2, %ymm1, %ymm1
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void

```



```

; register classes.

define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
%L34 = load i8, i8* %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246

CF246:
; preds = %CF246, %BB
%S1163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248

CF248:
; preds = %CF248, %CF246
store i8 %S1163, i8* %0
br label %CF248
}

```

## 1.9 clamav 0.102.4

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The basic library functions are written in C and are freestanding. Also included in the distribution is a set of C++ wrapper functions.

#### THE BASIC LIBRARY FUNCTIONS

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## 1.10 asnc1 0.9.24

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## 1.14 avflt 1.4

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When a "work that uses the Library" uses material from a header file that is part of the Library, the object code for the work may be a derivative work of the Library even though the source code is not. Whether this is true is especially significant if the work can be linked without the Library, or if the work is itself a library. The threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

You must give prominent notice with each copy of the work that the Library is used in it and that the Library and its use are covered by this License. You must supply a copy of this License. If the work during execution displays copyright notices, you must include the copyright notice for the Library among them, as well as a reference directing the user to the copy of this License. Also, you must do one of these things:

- a) Accompany the work with the complete corresponding machine-readable source code for the Library including whatever changes were used in the work (which must be distributed under Sections 1 and 2 above); and, if the work is an executable linked with the Library, with the complete machine-readable "work that uses the Library", as object code and/or source code, so that the user can modify the Library and then relink to produce a modified executable containing the modified Library. (It is understood that the user who changes the contents of definitions files in the

Library will not necessarily be able to recompile the application to use the modified definitions.)

b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

e) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

For an executable, the required form of the "work that uses the Library" must include any data and utility programs needed for reproducing the executable from it. However, as a special exception, the materials to be distributed need not include anything that is normally distributed (in either source or binary form) with the major components (compiler, kernel, and so on) of the operating system on which the executable runs, unless that component itself accompanies the executable.

It may happen that this requirement contradicts the license restrictions of other proprietary libraries that do not normally accompany the operating system. Such a contradiction means you cannot use both them and the Library together in an executable that you distribute.

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Sections above.

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library `Frob' (a library for tweaking knobs) written by James Random Hacker.

<signature of Ty Coon>, 1 April 1990  
Ty Coon, President of Vice

That's all there is to it!

## 1.19 curl 7.72.0

### 1.19.1 Available under license :

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License Mixing

=====

libcurl can be built to use a fair amount of various third party libraries,  
libraries that are written and provided by other parties that are distributed

using their own licenses. Even libcurl itself contains code that may cause problems to some. This document attempts to describe what licenses libcurl and the other libraries use and what possible dilemmas linking and mixing them all can lead to for end users.

I am not a lawyer and this is not legal advice!

One common dilemma is that [GPL](<https://www.gnu.org/licenses/gpl.html>) licensed code is not allowed to be linked with code licensed under the [Original BSD license](<https://spdx.org/licenses/BSD-4-Clause.html>) (with the announcement clause). You may still build your own copies that use them all, but distributing them as binaries would be to violate the GPL license - unless you accompany your license with an [exception](<https://www.gnu.org/licenses/gpl-faq.html#GPLIncompatibleLibs>). This particular problem was addressed when the [Modified BSD license](<https://opensource.org/licenses/BSD-3-Clause>) was created, which does not have the announcement clause that collides with GPL.

#### ## libcurl

Uses an [MIT style license](<https://curl.haxx.se/docs/copyright.html>) that is very liberal.

#### ## OpenSSL

(May be used for SSL/TLS support) Uses an Original BSD-style license with an announcement clause that makes it "incompatible" with GPL. You are not allowed to ship binaries that link with OpenSSL that includes GPL code (unless that specific GPL code includes an exception for OpenSSL - a habit that is growing more and more common). If OpenSSL's licensing is a problem for you, consider using another TLS library.

#### ## GnuTLS

(May be used for SSL/TLS support) Uses the [LGPL](<https://www.gnu.org/licenses/lgpl.html>) license. If this is a problem for you, consider using another TLS library. Also note that GnuTLS itself depends on and uses other libs (libgcrypt and libgpg-error) and they too are LGPL- or GPL-licensed.

#### ## WolfSSL

(May be used for SSL/TLS support) Uses the GPL license or a proprietary license. If this is a problem for you, consider using another TLS library.

#### ## NSS

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#### ## BoringSSL

(May be used for SSL/TLS support) As an OpenSSL fork, it has the same license as that.

#### ## libressl

(May be used for SSL/TLS support) As an OpenSSL fork, it has the same license as that.

#### ## BearSSL

(May be used for SSL/TLS support) Uses an MIT license that is very liberal and imposes no restrictions on any other library or part you may link with.

#### ## c-ares

(Used for asynchronous name resolves) Uses an MIT license that is very liberal and imposes no restrictions on any other library or part you may link with.

#### ## zlib

(Used for compressed Transfer-Encoding support) Uses an MIT-style license that shouldn't collide with any other library.

#### ## MIT Kerberos

(May be used for GSS support) MIT licensed, that shouldn't collide with any other parts.

#### ## Heimdal

(May be used for GSS support) Heimdal is Original BSD licensed with the

announcement clause.

## ## GNU GSS

(May be used for GSS support) GNU GSS is GPL licensed. Note that you may not distribute binary curl packages that uses this if you build curl to also link and use any Original BSD licensed libraries!

## ## libidn

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## ## OpenLDAP

(Used for LDAP support) Uses a Modified BSD-style license. Since libcurl uses OpenLDAP as a shared library only, I have not heard of anyone that ships OpenLDAP linked with libcurl in an app.

## ## libssh2

(Used for scp and sftp support) libssh2 uses a Modified BSD-style license.

# 1.20 util-linux 2.36-r0

## 1.20.1 Available under license :

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WEV @@ WEV[B "1

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NR START END SECTORS SIZE NAME UUID

1	32	7679	7648	3.7M	8f8378c0-01
2	7680	16383	8704	4.3M	8f8378c0-02
5	7936	12799	4864	2.4M	
6	12544	16127	3584	1.8M	

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Version 3, 29 June 2007

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```
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```

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```
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```

```
<signature of Ty Coon>, 1 April 1989
Ty Coon, President of Vice
```

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```
x ?"U@,5 @mISmIN<GimCN7g1u|E
43mI,5WEV @@ WEV @mImImIAmImImI0mImImI*mImI
A0mImImI...
lost+found...
```

```
;9GimCN7g
```

```
!"#$%&'()*+,-
./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~
```

```
!"#$%&'()*+,-
./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~
```

```
!"#$%&'()*+,-
./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~
```

```
!"#$%&'()*+,-
./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~WEV @@
WEV[B "1
```

## 1.21 libmspack 0.9.1alpha

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```

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```
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```

```
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Ty Coon, President of Vice
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## 1.22 sqlite 3.32.3

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```

# 1.23 clang 8.0.1

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-----

```
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\*/

; RUN: llc -march=hexagon < %s

; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types  
; cause LSR to assume type "void" for the memory type. This would then  
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8\*, i8, %union.anon.0 }

%union.anon.0 = type { i8\* }

define hidden fastcc void @fred() unnamed\_addr #0 {

entry:

br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph: ; preds = %entry

br label %while.body

while.body: ; preds = %exit.2, %while.body.lr.ph

%lsr.iv = phi %struct.0\* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]

switch i32 undef, label %exit [

i32 1, label %sw.bb.i

i32 2, label %sw.bb3.i

]

sw.bb.i: ; preds = %while.body

unreachable

sw.bb3.i: ; preds = %while.body

unreachable

exit: ; preds = %while.body

switch i32 undef, label %exit.2 [

i32 1, label %sw.bb.i17

i32 2, label %sw.bb3.i20

]

```

sw.bb.i17:                                ; preds = %.exit
%0 = bitcast %struct.0* %lshr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

sw.bb3.i20:                                ; preds = %exit
%2 = bitcast %struct.0* %lshr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable

exit.2:                                    ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lshr.iv, i32 1
br label %while.body

while.end:                                  ; preds = %entry
ret void
}

```

```
attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
```

---

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; NOTE: Assertions have been autogenerated by utils/update\_test\_checks.py UTC\_ARGS: --function-signature --scrub-attributes

; RUN: opt -S -passes='attributor' -aa-pipeline='basic-aa' -attributor-disable=false -attributor-max-iterations-verify -attributor-max-iterations=2 < %s | FileCheck %s

; Test that we only promote arguments when the caller/callee have compatible

; function attributes.

target triple = "x86\_64-unknown-linux-gnu"

; This should promote

```
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
```

```
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

```
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
```

```
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
```

```
; CHECK-NEXT: bb:
```

```
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
```

```
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
```

```
; CHECK-NEXT: ret void
```

```
;
```

```
bb:
```

```
  %tmp = load <8 x i64>, <8 x i64>* %arg1
```

```
  store <8 x i64> %tmp, <8 x i64>* %arg
```

```
  ret void
```

```
}
```

```
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
```

```
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

```
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
```

```
; CHECK-NEXT: bb:
```

```
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
```

```
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
```

```
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
```

```
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
```

```
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
```

```

; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias
nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void

```

```

;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x
i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias
nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32

```

```

%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x
i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias
nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)

```

```

call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; This should not promote

```

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{{^@+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias
nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32

```



```

store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #2 {
; CHECK-LABEL: define {{{^@+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x
i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias
nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

```

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define {{{^@+}}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>*
noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture
nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8

```

```

x i64>* readonly %arg1) #4 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
; CHECK-LABEL: define {{{^@}+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64
32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>*
noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture
nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }

```

```
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-  
width"="512" "prefer-vector-width"="256" }  
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-  
width"="256" "prefer-vector-width"="256" }  
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"  
"prefer-vector-width"="256" }  
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"  
"prefer-vector-width"="256" }  
attributes #5 = { argmemonly nounwind }
```

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```
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s
```

```
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {  
; CHECK-LABEL: test_sitofp_fixed:
```

```
; First, extend each i32 to i64
```

```
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
```

```
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
```

```
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
```

```
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
```

```
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
```

```
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
```

```
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
```

```
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
```

```
; Next, convert each to double.
```

```
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
```

```
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
```

```
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
```

```
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
```

```
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
```

```
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
```

```
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
```

```
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]
```

```
; CHECK: ret
```

```
%flt = sitofp <16 x i32> %in to <16 x double>
```

```
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,  
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
```



```

double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

```

---

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; NOTE: Assertions have been autogenerated by utils/update\_test\_checks.py UTC\_ARGS: --function-signature --scrub-attributes

; RUN: opt -S -argpromotion < %s | FileCheck %s

; RUN: opt -S -passes=argpromotion < %s | FileCheck %s

; Test that we only promote arguments when the caller/callee have compatible

; function attributes.

target triple = "x86\_64-unknown-linux-gnu"

; This should promote

```
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
```

```
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

```
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
```

```
; CHECK-NEXT: bb:
```

```
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
```

```
; CHECK-NEXT: ret void
```

```
;
```

```
bb:
```

```
%tmp = load <8 x i64>, <8 x i64>* %arg1
```

```
store <8 x i64> %tmp, <8 x i64>* %arg
```

```
ret void
```

```
}
```

```
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
```

```
; CHECK-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

```
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
```

```
; CHECK-NEXT: bb:
```

```
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
```

```
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
```

```
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
```

```
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
```

```
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
```

```
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
```

```
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
```

```
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
```

```
; CHECK-NEXT: ret void
```

```
;
```

```
bb:
```

```
%tmp = alloca <8 x i64>, align 32
```

```

%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; This should promote

```

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32

```



```

store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,

```

```

<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]

```

```

; CHECK-NEXT:  ret void
;
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{{^@+}}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #2 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT:  ret void
;
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void

```

```

}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x
i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define {{{^@+}}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

```

```

; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #4 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
; CHECK-LABEL: define {{{^@+}}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])

```

```

; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdetsiz
define i32 @f20(double %a) strictfp {
entry:
%result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                        metadata !"fpexcept.strict")
                        strictfp

ret i32 %result
}

```

```

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

```

```

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

```

```

define fp128 @TestSelect(fp128 %a, fp128 %b) {
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
  ret fp128 %res
; CHECK-LABEL: TestSelect:
; CHECK    movaps 16(%rsp), %xmm1
; CHECK-NEXT callq __subtf3
; CHECK-NEXT testl %ebx, %ebx
; CHECK-NEXT jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT addq $32, %rsp
; CHECK-NEXT popq %rbx
; CHECK-NEXT retq
}

```

```

define fp128 @TestFabs(fp128 %a) {
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
; CHECK-LABEL: TestFabs:
; CHECK    andps .LCPI1_0(%rip), %xmm0
; CHECK-NEXT retq
}

```

```

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
  ret fp128 %res
; CHECK-LABEL: TestCopysign:
; CHECK    andps .LCPI2_1(%rip), %xmm0
; CHECK-NEXT orps %xmm1, %xmm0
; CHECK-NEXT retq
}

```

```

define fp128 @TestFneg(fp128 %a) {
  %mul = fmul fp128 %a, %a

```

```

%res = fsub fp128 0xL00000000000000008000000000000000, %mul
ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK    movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-
prefixes=CHECK,VEC256,AVX
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-
prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256("min-legal-vector-width"="256" {
; VEC256-LABEL: 'zext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>

```



```

%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

```

```

define void @sext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'sext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

```

```

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

```

```

;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}
# People who have agreed to one of the CLAs and can contribute patches.
# The AUTHORS file lists the copyright holders; this file
# lists people. For example, Google employees are listed here
# but not in AUTHORS, because Google holds the copyright.
#
# Names should be added to this file only after verifying that
# the individual or the individual's organization has agreed to
# the appropriate Contributor License Agreement, found here:
#
# https://developers.google.com/open-source/cla/individual
# https://developers.google.com/open-source/cla/corporate

```

#  
# The agreement for individuals can be filled out on the web.  
#  
# When adding J Random Contributor's name to this file,  
# either J's name or J's organization's name should be  
# added to the AUTHORS file, depending on whether the  
# individual or corporate CLA was used.  
#  
# Names should be added to this file as:  
# Name <email address>  
#  
# Please keep the list sorted.

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Zbigniew Skowron <zbychs@gmail.com>  
; RUN: opt -consthoist -S -o - %s | FileCheck %s  
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"  
target triple = "thumbv6m-none--musleabi"

```
; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo
```

```
@goo = global i8* undef
```

```
define void @foo_i8() {
```

```

entry:
%0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
%1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
%2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
%3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
%4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

```

; Check that for i16 type, the maximum legal offset is 62.

```

; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

```

```

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}

```

; Check that for i32 type, the maximum legal offset is 124.

```

; CHECK: foo_i32

```

```

; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4

```

```
define void @foo_i32() {
```

```
entry:
```

```

%0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
%1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
%2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
%3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
%4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
%5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
ret void
}

```

```
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
```

```
;
```

```
; Test that early if conversion produces LOCR with operands of the right
```

```
; register classes.
```

```
define void @autogen_SD4739(i8*) {
```

```
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
```

```
BB:
```

```

%L34 = load i8, i8* %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246

```

```
CF246:                                ; preds = %CF246, %BB
```

```

%SI163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248

```

```
CF248:                                ; preds = %CF248, %CF246
```

```

store i8 %SI163, i8* %0
br label %CF248

```

```
}  
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py  
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s
```

; A shuffle mask with all undef elements is always legal.

```
define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {  
; CHECK-LABEL: PR41535:  
; CHECK:      // %bb.0:  
; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4  
; CHECK-NEXT:  mov v0.d[1], v0.d[0]  
; CHECK-NEXT:  ret  
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>  
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>  
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>  
ret <4 x i32> %r  
}
```

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; NOTE: Assertions have been autogenerated by utils/update\_llc\_test\_checks.py

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpadd

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; RUN: llc < %s -mtriple=x86\_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```
define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: add256:
```

```
; CHECK:      # %bb.0:
```

```
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
```

```
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
```

```
; CHECK-NEXT:  vpadd 32(%rsi), %ymm1, %ymm1
```

```
; CHECK-NEXT:  vpadd (%rsi), %ymm0, %ymm0
```





```

%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-
width"="512" {

```

```

; CHECK-LABEL: pmaddwd_32_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-
width"="256" {

```

```

; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <64 x i8>, <64 x i8>* %xptr

```

```

%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB8_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT: vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT: vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT: vpadd %ymm1, %ymm3, %ymm1
; CHECK-NEXT: vpmovsxbw 16(%rsi,%rcx), %ymm3
; CHECK-NEXT: vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT: vpadd %ymm2, %ymm3, %ymm2
; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax

```

```

; CHECK-NEXT:   jne .LBB8_1
; CHECK-NEXT:   # %bb.2: # %middle.block
; CHECK-NEXT:   vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:   vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:   vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:   vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:   vpslufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:   vpslufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:   vmovd %xmm0, %eax
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq

```

entry:

```

%3 = zext i32 %2 to i64
br label %vector.body

```

vector.body:

```

%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

```

middle.block:

```

%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef>

```

```

i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

```

```

define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-
width"="512" {

```

```

; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB9_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT: vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT: vpadd %zmm1, %zmm2, %zmm1
; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax
; CHECK-NEXT: jne .LBB9_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT: vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

```

entry:

```
%3 = zext i32 %2 to i64  
br label %vector.body
```

vector.body:

```
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]  
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]  
%4 = getelementptr inbounds i8, i8* %0, i64 %index  
%5 = bitcast i8* %4 to <32 x i8>*  
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1  
%6 = sext <32 x i8> %wide.load to <32 x i32>  
%7 = getelementptr inbounds i8, i8* %1, i64 %index  
%8 = bitcast i8* %7 to <32 x i8>*  
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1  
%9 = sext <32 x i8> %wide.load14 to <32 x i32>  
%10 = mul nsw <32 x i32> %9, %6  
%11 = add nsw <32 x i32> %10, %vec.phi  
%index.next = add i64 %index, 32  
%12 = icmp eq i64 %index.next, %3  
br i1 %12, label %middle.block, label %vector.body
```

middle.block:

```
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,  
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32  
undef, i32 undef, i32 undef>  
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1  
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32  
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>  
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf  
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32  
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32  
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>  
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15  
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32  
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32  
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>  
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17  
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32  
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,  
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>  
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19  
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
```



```
ret i32 %13
}
```

@a = global [1024 x i8] zeroinitializer, align 16

@b = global [1024 x i8] zeroinitializer, align 16

```
define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: sad_16i8_256:
```

```
; CHECK: # %bb.0: # %entry
```

```
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
```

```
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
```

```
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
```

```
; CHECK-NEXT: .p2align 4, 0x90
```

```
; CHECK-NEXT: .LBB10_1: # %vector.body
```

```
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
```

```
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
```

```
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
```

```
; CHECK-NEXT: vpadd %ymm1, %ymm2, %ymm1
```

```
; CHECK-NEXT: addq $4, %rax
```

```
; CHECK-NEXT: jne .LBB10_1
```

```
; CHECK-NEXT: # %bb.2: # %middle.block
```

```
; CHECK-NEXT: vpadd %ymm0, %ymm1, %ymm0
```

```
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vpsltd {.*#+} xmm1 = xmm0[2,3,0,1]
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vpsltd {.*#+} xmm1 = xmm0[1,1,2,3]
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vmovd %xmm0, %eax
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
entry:
```

```
br label %vector.body
```

```
vector.body:
```

```
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
```

```
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
```

```
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
```

```
%1 = bitcast i8* %0 to <16 x i8>*
```

```
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
```

```
%2 = zext <16 x i8> %wide.load to <16 x i32>
```

```
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
```

```
%4 = bitcast i8* %3 to <16 x i8>*
```

```
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
```

```
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
```

```
%6 = sub nsw <16 x i32> %2, %5
```

```
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
```

```

%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

```

middle.block:

```

%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12,
i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

```

```

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-LABEL: sad_16i8_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB11_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT: vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB11_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT: vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpslufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0

```

```

; CHECK-NEXT: vpsfud {.*#+} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
br label %vector.body

vector.body:
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12

```

```

}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  kshiftrw $8, %k0, %k1
; CHECK-NEXT:  vpmovm2d %k1, %ymm0
; CHECK-NEXT:  vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:  vpmovm2d %k0, %ymm1
; CHECK-NEXT:  vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:  vmovaps %ymm1, (%rdi)
; CHECK-NEXT:  vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  kshiftrw $8, %k0, %k1
; CHECK-NEXT:  vpmovm2d %k1, %ymm0
; CHECK-NEXT:  vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:  vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:  vpmovm2d %k0, %ymm2
; CHECK-NEXT:  vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:  vextracti128 $1, %ymm2, %xmm2

```

```

; CHECK-NEXT:   vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:   vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:   vmovaps %ymm3, (%rdi)
; CHECK-NEXT:   vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:   vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:  vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:  vmovaps %zmm1, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  kshiftrw $8, %k0, %k1
; CHECK-NEXT:  vpmovm2d %k1, %ymm0
; CHECK-NEXT:  vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:  vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:  vpmovm2d %k0, %ymm1
; CHECK-NEXT:  vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT:  vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:  vmovaps %ymm1, (%rdi)
; CHECK-NEXT:  vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>

```

```

store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {

```

```

; CHECK-LABEL: ubto16f64_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm1, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {

```

```

; CHECK-LABEL: test_16f32toub_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k0
; CHECK-NEXT: vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {

```

```

; CHECK-LABEL: test_16f32toub_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>

```

```

%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:    # %bb.0:
; CHECK-AVX512-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-AVX512-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-AVX512-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %ymm4 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13
],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ym
m0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[
31]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %ymm5 =

```



```

ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13
],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm
m0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[
31]
; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT: vmovdqa {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[
5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[
19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[
5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[
19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm3 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13
],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm
m0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[
31]
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm3, %ymm3
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[
5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[
19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovdqa 32(%rsi), %ymm3

```

```

; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13
],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm
m0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[
31]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13
],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm
m0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[
31]
; CHECK-VBMI-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[
5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[
19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[
5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[
19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-VBMI-NEXT:  vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13
],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm
m0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[
31]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm2 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[
5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[
19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm0
; CHECK-VBMI-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-VBMI-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void

```

}

```
define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-AVX512-LABEL: mul512:
; CHECK-AVX512:    # %bb.0:
; CHECK-AVX512-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0
[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],z
mm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[
45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],z
mm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[
63]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vmovdqa64 {{.*#+}} zmm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,2
55,255,255,255,255]
; CHECK-AVX512-NEXT:  vpandq %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
zmm1[0],zmm0[0],zmm1[1],zmm0[1],zmm1[2],zmm0[2],zmm1[3],zmm0[3],zmm1[4],zmm0[4],zmm1[5],zmm0[5]
,zmm1[6],zmm0[6],zmm1[7],zmm0[7],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19]
,zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[32],zmm
0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],zmm1[37],zmm0[37],
zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1
[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpandq %zmm3, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:    # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0
[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],z
```

```

mm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[
45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],z
mm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[
63]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
zmm1[0],zmm0[0],zmm1[1],zmm0[1],zmm1[2],zmm0[2],zmm1[3],zmm0[3],zmm1[4],zmm0[4],zmm1[5],zmm0[5]
,zmm1[6],zmm0[6],zmm1[7],zmm0[7],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19]
,zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[32],zmm
0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],zmm1[37],zmm0[37],
zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1
[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 {{.*#+}} zmm1 =
[0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,
46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]
; CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-
width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT:  vblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT:  retq
%mask = icmp eq <4 x i32> %trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32>
%dst)
ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* , i32, <4 x i1>, <4 x i32>)

```

```

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
; CHECK-NEXT: vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT: vpmovqd %ymm2, %xmm1
; CHECK-NEXT: vpmovqd %ymm3, %xmm2
; CHECK-NEXT: vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}

```

```

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqb %ymm3, %xmm3
; CHECK-NEXT: vpmovqb %ymm2, %xmm2
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm2[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

```

```

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0]

```

```

; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqb %ymm1, %xmm1
; CHECK-NEXT:  vpmovqb %ymm0, %xmm0
; CHECK-NEXT:  vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqw %ymm1, %xmm1
; CHECK-NEXT:  vpmovqw %ymm0, %xmm0
; CHECK-NEXT:  vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i16>
ret <8 x i16> %b
}

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm2
; CHECK-NEXT:  vmovdqa {{.*#+}} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]
; CHECK-NEXT:  vpermi2w %ymm1, %ymm2, %ymm0
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
}

```







```

o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xm
m0[15],zero
; CHECK-NEXT: vpslufd {{.*#+}} xmm2 = xmm1[2,3,0,1]
; CHECK-NEXT: vpmovzxdq {{.*#+}} ymm2 =
xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpslufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT: vpmovzxdq {{.*#+}} ymm3 =
xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT: vpmovzxdq {{.*#+}} ymm1 =
xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT: vpmovzxbd {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,zero,zero,zero,zero,xmm0[1],zero,zero,zero,zero,zero,zero,zero,xmm0[2],zero,zero,zero,zer
o,zero,zero,zero,xmm0[3],zero,zero,zero,zero,zero,zero,zero,zero,zero,zero
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

```

```

define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovsxbd %xmm0, %ymm0
; CHECK-NEXT: vpslufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpmovsxdq %xmm1, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm2
; CHECK-NEXT: vpslufd {{.*#+}} xmm3 = xmm2[2,3,0,1]
; CHECK-NEXT: vpmovsxdq %xmm3, %ymm3
; CHECK-NEXT: vpmovsxdq %xmm0, %ymm0
; CHECK-NEXT: vpmovsxdq %xmm2, %ymm2
; CHECK-NEXT: vmovdqa %ymm2, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

```

```

define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>*

```

```

%r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

```

```

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>*
%r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqd %ymm1, %ymm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

```

```

define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x
i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2

```

```

; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

```

```

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i16> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

```

```

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: vpmovuswb %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

```

```

%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
ret <16 x i8> %f
}

```

```

define void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256"
{
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: vpmovuswb %ymm0, (%rsi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

```

```

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:      # %bb.0:
; CHECK-NEXT: retq
ret <64 x i1> %x
}

```

```

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT: vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT: kshiftrd $1, %k0, %k1
; CHECK-NEXT: movq $-3, %rax

```

```

; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftlq $63, %k0, %k2
; CHECK-NEXT: kshiftrq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-5, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $3, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $61, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-9, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $2, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $60, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-17, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $5, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $59, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $4, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $58, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $7, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $57, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-129, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $6, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $56, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-257, %rax # imm = 0xFEFF

```

```

; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $9, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $55, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-513, %rax # imm = 0xFDFD
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $8, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $54, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $11, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $53, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $10, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $52, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $13, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $51, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $12, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $50, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $15, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $49, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1

```

```

; CHECK-NEXT: movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $14, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $48, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65537, %rax # imm = 0xFFFFEFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $17, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $47, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-131073, %rax # imm = 0xFFFDFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $16, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $46, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-262145, %rax # imm = 0xFFFBFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $19, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $45, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-524289, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $18, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $44, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1048577, %rax # imm = 0xFFEFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $21, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $43, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $20, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $42, %k2, %k2

```

```

; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4194305, %rax # imm = 0xFFBFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $23, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $41, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8388609, %rax # imm = 0xFF7FFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $22, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $40, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16777217, %rax # imm = 0xFEFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $25, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $39, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $24, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $38, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $27, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $37, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $26, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $36, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $29, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2

```



```

; CHECK-NEXT: kshiftrq $35, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $28, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $34, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $31, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $33, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k2
; CHECK-NEXT: vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT: kshiftrd $30, %k0, %k0
; CHECK-NEXT: kshiftlq $63, %k0, %k0
; CHECK-NEXT: kshiftrq $32, %k0, %k0
; CHECK-NEXT: korq %k0, %k2, %k0
; CHECK-NEXT: movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $1, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftlq $63, %k1, %k2
; CHECK-NEXT: kshiftrq $30, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $3, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $29, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-34359738369, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $2, %k1, %k2

```

```

; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $28, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-68719476737, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $5, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $27, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-137438953473, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $4, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $26, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-274877906945, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $7, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $25, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-549755813889, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $6, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $24, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1099511627777, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $9, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $23, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2199023255553, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $8, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $22, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4398046511105, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0

```

```

; CHECK-NEXT: kshiftrd $11, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $21, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8796093022209, %rax # imm = 0xFFFFF7FFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $10, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $20, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17592186044417, %rax # imm = 0xFFFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $13, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $19, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-35184372088833, %rax # imm = 0xFFFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $12, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $18, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-70368744177665, %rax # imm = 0xFFFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $15, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $17, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-140737488355329, %rax # imm = 0xFFFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $14, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $16, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-281474976710657, %rax # imm = 0xFFFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $17, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $15, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-562949953421313, %rax # imm = 0xFFFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2

```

```

; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $16, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $14, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1125899906842625, %rax # imm = 0xFFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $19, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $13, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2251799813685249, %rax # imm = 0xFFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $18, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $12, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4503599627370497, %rax # imm = 0xFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $21, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $11, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-9007199254740993, %rax # imm = 0xFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $20, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $10, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $23, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $9, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-36028797018963969, %rax # imm = 0xFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $22, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $8, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-72057594037927937, %rax # imm = 0xFEFFFFFFFFFFFFFFF

```

```

; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $25, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $7, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-144115188075855873, %rax # imm = 0xFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $24, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $6, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-288230376151711745, %rax # imm = 0xFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $27, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $5, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-576460752303423489, %rax # imm = 0xF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $26, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $4, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $29, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $3, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2305843009213693953, %rax # imm = 0xDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $28, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $2, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4611686018427387905, %rax # imm = 0xBF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $31, %k1, %k2
; CHECK-NEXT: kshiftrlq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $30, %k1, %k1

```

```

; CHECK-NEXT: kshiftrlq $1, %k0, %k0
; CHECK-NEXT: kshiftrq $1, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k1, %k1
; CHECK-NEXT: korq %k1, %k0, %k1
; CHECK-NEXT: vmovdqu8 %ymm1, (%rsi) {%k1}
; CHECK-NEXT: kshiftrq $32, %k1, %k1
; CHECK-NEXT: vmovdqu8 %ymm0, 32(%rsi) {%k1}
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32
6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32
22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39,
i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32
55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 1, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = global i64 0, align 8
@mem64_src = global i64 0, align 8
define i32 @v64i1_inline_asm("min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK: # %bb.0:
; CHECK-NEXT: kmovq {{.*}}(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, {{.*}}(%rip)
; CHECK-NEXT: movl -{{[0-9]++}}(%rsp), %eax
; CHECK-NEXT: retq
%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 @asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall("min-legal-vector-width"="128" {
ret void
}

define internal void @innerLarge("min-legal-vector-width"="512" {
ret void
}

```

```

}

define internal void @innerNoAttribute() {
  ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

```

## 1.24 jansson 2.11

### 1.24.1 Available under license :

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